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Haratsch 1-4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Erich Franz Haratsch, Harish Viswanathan
Case: 1-4
Serial No.: 09/326,785
Filing Date: June 4, 1999
Title: Method and Apparatus for Reducing the Computational Complexity and Relaxing the Critical Path of Reduced State Sequence Estimation (RSSE) Techniques

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant's attorney wishes to bring to the attention of the Patent and Trademark Office the following documents listed on the accompanying PTO Form 1449. A copy of each listed item is enclosed.

5. S.L. Ariyavisitakul and Ye Li, "Joint Coding and Decision Feedback Equalization for Broadband Wireless Channels," IEEE Journal on Selected Areas in Communications, Vol. 16, No. 9, 1670-78 (Dec. 1998);
6. G. Fettweis and H. Meyr, "High-Speed Parallel Viterbi Decoding: Algorithm and VLSI-Architecture," IEEE Communications Magazine, 46-55 (May, 1991); and
7. N. Seshadri and J.B. Anderson, "Decoding of Severely Filtered Modulation Codes Using the (M, L) Algorithm," IEEE Journal on Selected Areas in Communications, Vol. 7, No. 6, 1006-1016 (Aug. 1989).

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability or that no other material information exists.

Respectfully submitted,



Date: August 24, 1999

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